IN THE CLAIMS:

Please note that all claims currently pending and under consideration in the referenced application are shown below, in clean form, for clarity. No Amendments to the claims have been made.

1. A DRAM circuit comprising:

a substrate having a capacitor structure disposed thereon, said capacitor structure including a storage node, a dielectric layer overlying said storage node, and a conductive cell plate overlying said dielectric layer, each of said dielectric layer and said conductive cell plate having an end portion;

a conductive contact extending downward and adjacently beside said capacitor structure, said end portion of said dielectric layer extending closer to said conductive contact than said end portion of said conductive cell plate; and

a TEOS layer disposed over said capacitor structure and encasing said end portions of said dielectric layer and said conductive cell plate, said TEOS layer disposed between said capacitor structure and said conductive contact.

2. The DRAM circuit of claim 1, further comprising an insulating layer disposed over said TEOS layer, said conductive contact extending through said insulating layer and said TEOS layer.

3. The DRAM circuit of claim 2, wherein said insulating layer comprises a heavily doped BPSG layer.

4. The DRAM circuit of claim 1, wherein each of said storage node and said conductive cell plate are heavily doped with dopants.

5. The DRAM circuit of claim 1, wherein each of said storage node and said conductive cell plate comprise a phosphorous-doped polysilicon.

6. The DRAM circuit of claim 1, wherein said dielectric layer comprises a capacitor cell dielectric layer.

7. The DRAM circuit of claim 1, wherein said dielectric layer comprises a nitride layer.

8. The DRAM circuit of claim 1, wherein said capacitor structure comprises a container-shaped capacitor.

9. (Previously Amended) The DRAM circuit of claim 2, wherein said TEOS layer comprises a dopant barrier between said capacitor structure and said insulating layer.

10. (Previously Amended) A semiconductor memory device comprising:

a semiconductor substrate having a capacitor structure formed thereon, said capacitor structure including a first conductive layer, a second conductive layer, and a dielectric layer, said dielectric layer disposed between said first and second conductive layers, each of said dielectric layer and said first and second conductive layers having an end portion;

a conductive contact extending downward and adjacently beside said capacitor structure, said end portion of said dielectric layer extending closer to said conductive contact than said end portion of each of said first conductive layer and said second conductive layer; and

a TEOS layer disposed over said capacitor structure and encasing said end portions of said dielectric layer and each of said first conductive layer and said second conductive layer, said TEOS layer disposed between said capacitor structure and said conductive contact.

11. The device of claim 10, further comprising an insulating layer disposed over said TEOS layer, said conductive contact extending through said insulating layer and said TEOS layer.

12. The device of claim 11, wherein said insulating layer comprises a heavily doped BPSG layer.

13. The device of claim 10, wherein said conductive contact comprises at least one of metal and conductively doped polysilicon.

14. The device of claim 10, wherein said conductive contact comprises a digit line.

15. The device of claim 10, wherein each of said first conductive layer and said second conductive layer are heavily doped with dopants.

16. The device of claim 10, wherein each of said first conductive layer and said second conductive layer comprise a phosphorous-doped polysilicon.

17. The device of claim 10, wherein said dielectric layer comprises a capacitor cell dielectric layer.

18. The device of claim 10, wherein said dielectric layer comprises a nitride layer.

19. The device of claim 10, wherein said capacitor structure comprises a container-shaped capacitor.

20. (Previously Amended) The device of claim 11, wherein said TEOS layer comprises a dopant barrier between said capacitor structure and said insulating layer.